

# **aP58Q6**

**18 minutes voice erasable chip**

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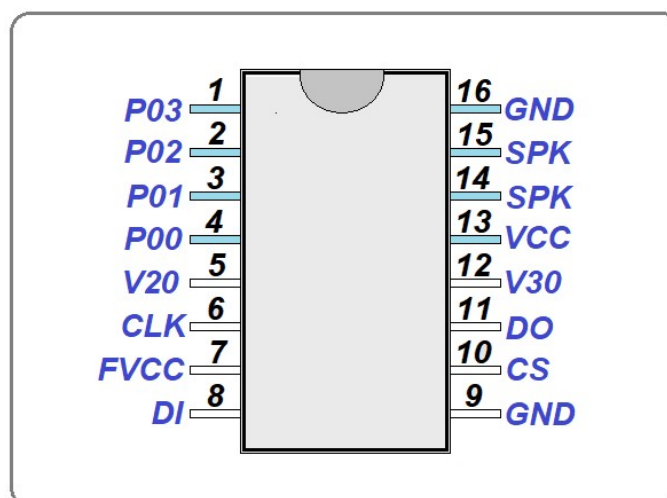
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**■ Features :**

- Built in 8-bit DSP
- System CPU clock :24MHz
- Program memory : 512k bits(64 K Bytes) OTP.
- Voice memory : 32M bits(4M Bytes) FLASH memory
- 1080 sec voice length at 5.8KHz sampling or 276 sec voice length at 23KHz sampling.
- Built-in 2k bits(256 Bytes) SRAM.
- Built-in R/C Trim ( 1% )
- Built-in 1 set PWM and 1 set DAC..
- GPIO x 4 available
- Built in low voltage detection and reset system circuit (LVR)
- Built-in Watch Dog Timer.
- Optional PWM driving ability : High Middle Low Buffer Drive .
- Operating Voltage Range: 2.3V ~ 5.0V.
- Five standard triggering modes are available
  - SBT mode
  - Matrix key
  - Cpu serial 1-wire mode
  - Cpu serial 2-wire mode
  - Cpu serial 3-wire mode



<b>Duration Table</b>					
<b>Coding</b>	<b>AD5</b>	<b>AD6</b>	<b>AD8</b>	<b>PCM10</b>	<b>PCM12</b>
<b>SR = 4.6K</b>	<b>23 min.</b>	<b>19.4 min.</b>	<b>14.5 min.</b>	<b>11.6 min.</b>	<b>9.7 min.</b>
<b>SR = 5.8K</b>	<b>18.6 min.</b>	<b>15.5 min.</b>	<b>11.6 min.</b>	<b>9.3 min.</b>	<b>7.7 min.</b>
<b>SR = 6.6K</b>	<b>16.3 min.</b>	<b>13.5 min.</b>	<b>10.1 min.</b>	<b>8.1 min.</b>	<b>6.7 min.</b>
<b>SR = 7.8K</b>	<b>13.9 min.</b>	<b>11.6 min.</b>	<b>8.7 min.</b>	<b>6.9 min.</b>	<b>5.8 min.</b>
<b>SR = 9.3K</b>	<b>11.6 min.</b>	<b>9.7 min.</b>	<b>7.2 min.</b>	<b>5.8 min.</b>	<b>4.8 min.</b>
<b>SR = 11.7K</b>	<b>9.3 min.</b>	<b>7.7 min.</b>	<b>5.8 min.</b>	<b>4.6 min.</b>	<b>3.8 min.</b>
<b>SR = 15.6K</b>	<b>6.9 min.</b>	<b>5.8 min.</b>	<b>4.3 min.</b>	<b>3.4 min.</b>	<b>2.9 min.</b>
<b>SR = 23.4K</b>	<b>4.6 min.</b>	<b>3.8 min.</b>	<b>2.9 min.</b>	<b>2.3 min.</b>	<b>1.9 min.</b>

■ **PIN NAMES :**

<b>Pin No.</b>	<b>Designation</b>	<b>I/O</b>	<b>Description</b>
<b>1</b>	<b>P0[3] / Reset</b>	<b>I/O</b>	<b>Port-0 I/O.</b>
<b>2</b>	<b>P0[2]</b>	<b>I/O</b>	<b>Port-0 I/O.</b>
<b>3</b>	<b>P0[1]</b>	<b>I/O</b>	<b>Port-0 I/O</b>
<b>4</b>	<b>P0[0]</b>	<b>I/O</b>	<b>Port-0 I/O</b>
<b>5</b>	<b>V20</b>	<b>P</b>	<b>Digital Power. ( LDO 2V output ).</b>
<b>6</b>	<b>CLK</b>	<b>I/O</b>	<b>CLK of SPI FLASH</b>
<b>7</b>	<b>FVCC</b>	<b>P</b>	<b>Power of SPI FLASH</b>
<b>8</b>	<b>DI</b>	<b>I/O</b>	<b>DI of SPI FLASH</b>
<b>9</b>	<b>GND</b>	<b>P</b>	<b>System Ground.</b>
<b>10</b>	<b>CS</b>	<b>I/O</b>	<b>CS of SPI FLASH</b>
<b>11</b>	<b>DO</b>	<b>I/O</b>	<b>DO of SPI FLASH</b>
<b>12</b>	<b>V30</b>	<b>P</b>	<b>IO Power. ( LDO 3V output ).</b>
<b>13</b>	<b>VCC</b>	<b>P</b>	<b>Chip Power.</b>
<b>14</b>	<b>SPK_P</b>	<b>O</b>	<b>DAC / PWM1</b>
<b>15</b>	<b>SPK_N</b>	<b>O</b>	<b>PWM2</b>
<b>16</b>	<b>GND</b>	<b>P</b>	<b>System Ground.</b>

**Group Options :**

Selectable options that affect each individual group are called Group Options. They are:  
 Edge or Level trigger.  
 Unholdable or Holdable  
 Re-trigger or Non-retrigger  
 Stop pulse disable or enable.

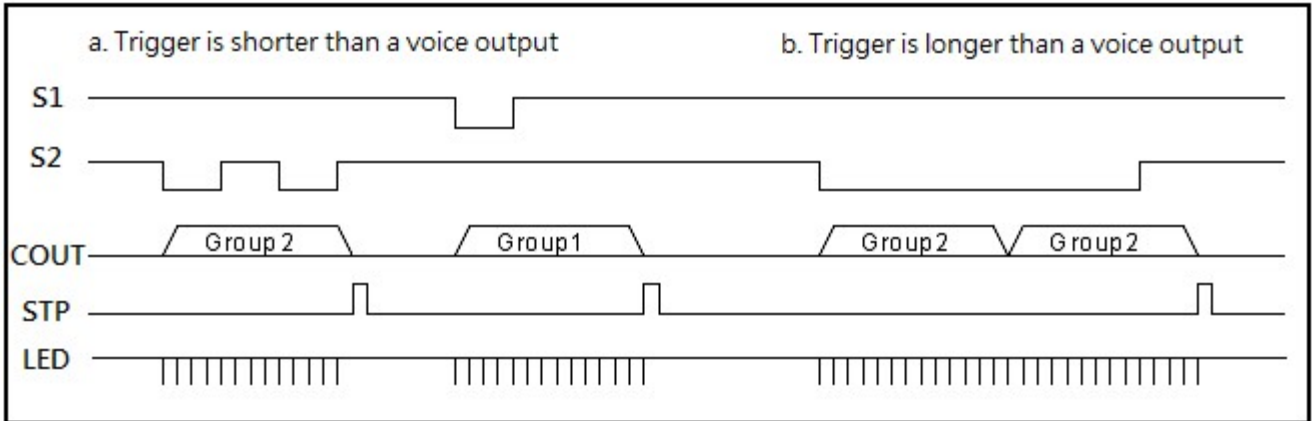


Fig. 1 Level, Unholdable, Non-retrigger

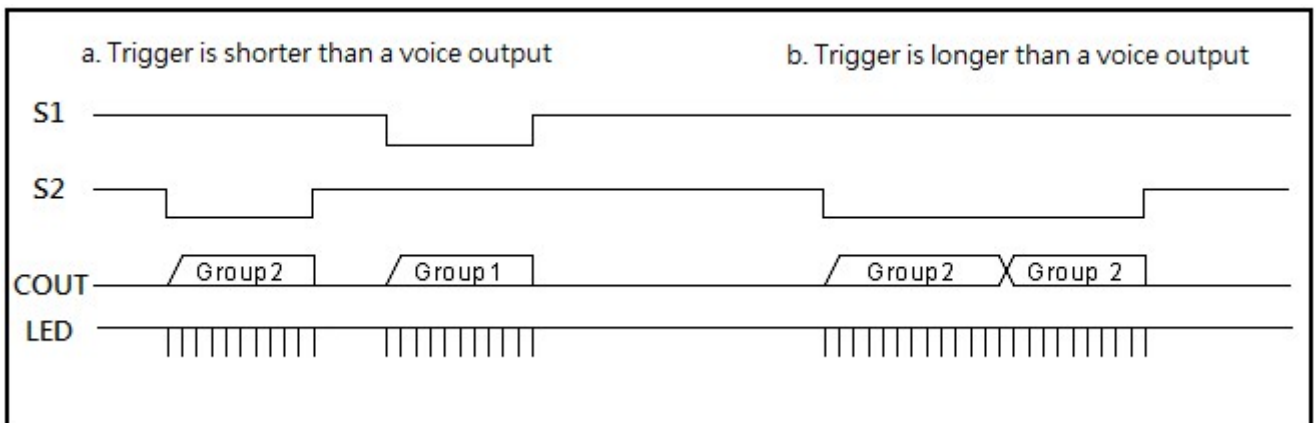


Fig. 2 Level Holdable

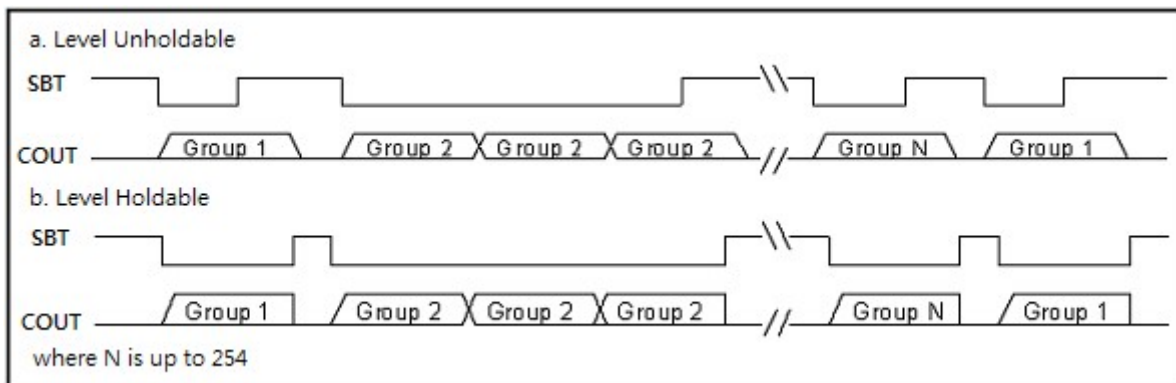


Fig. 3 SBT sequential trigger with Level Holdable and Unholdable

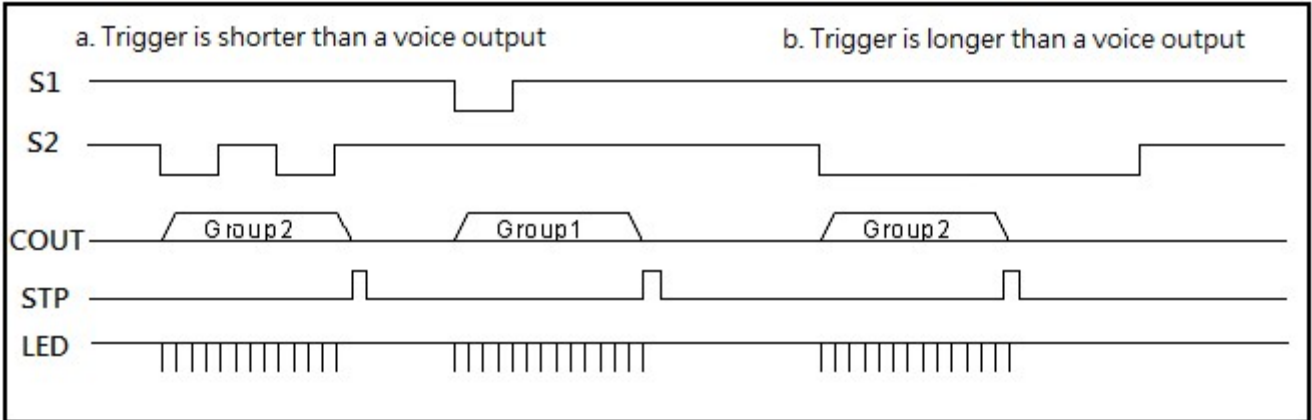


Fig. 4 Edge, Unholdable, Non-retrigger

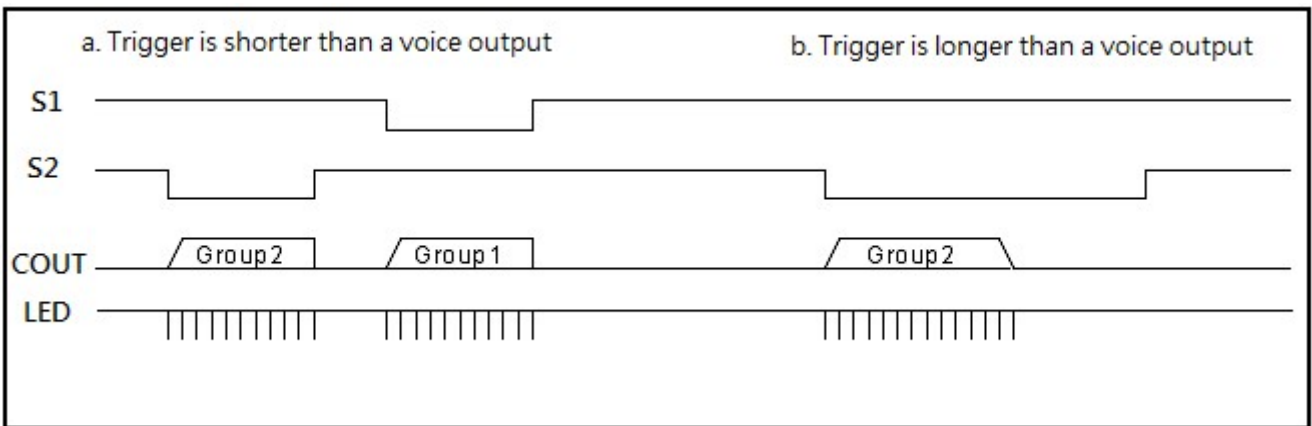


Fig. 5 Edge, Holdable

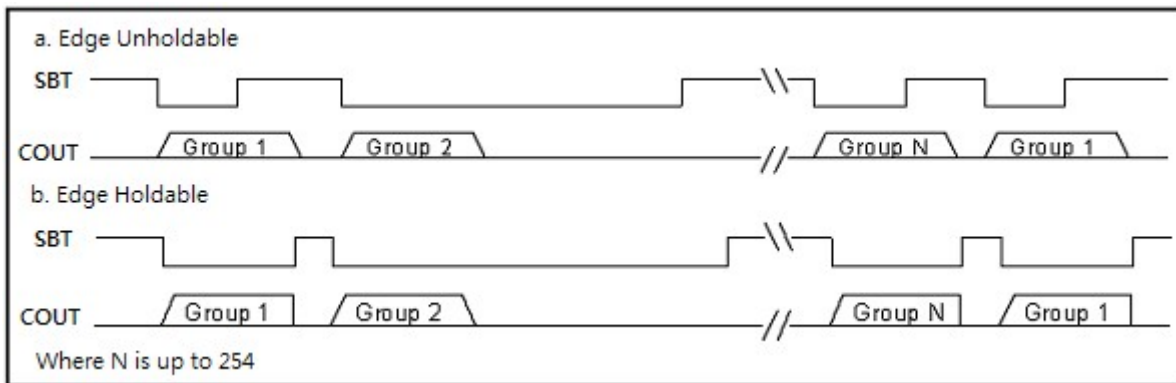


Fig. 6 SBT sequential trigger with Edge Holdable and Unholdable

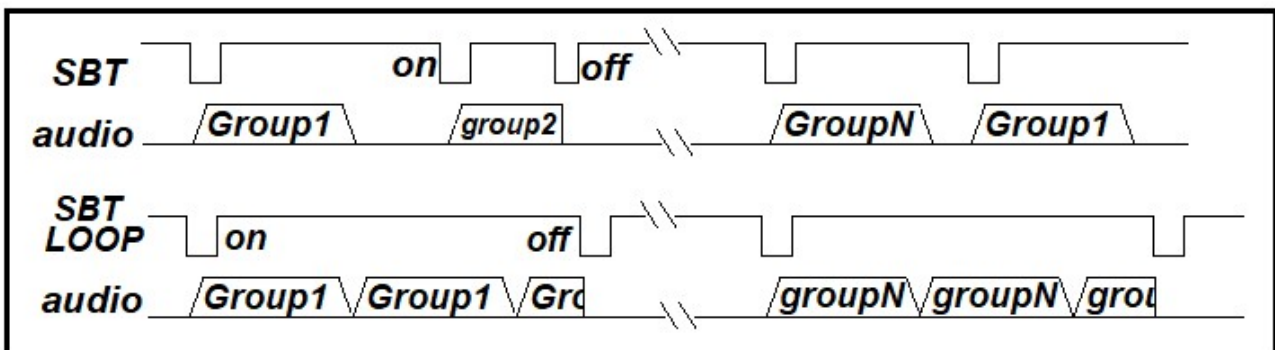


Fig. 7 SBT sequential trigger with On/Off

● **Trigger mode :**

1. **SBT mode :**

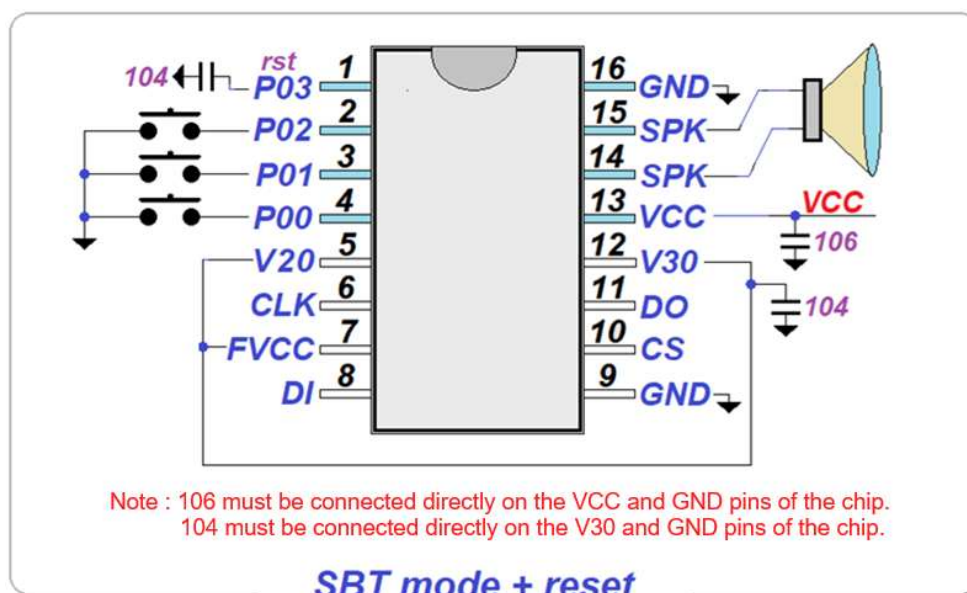
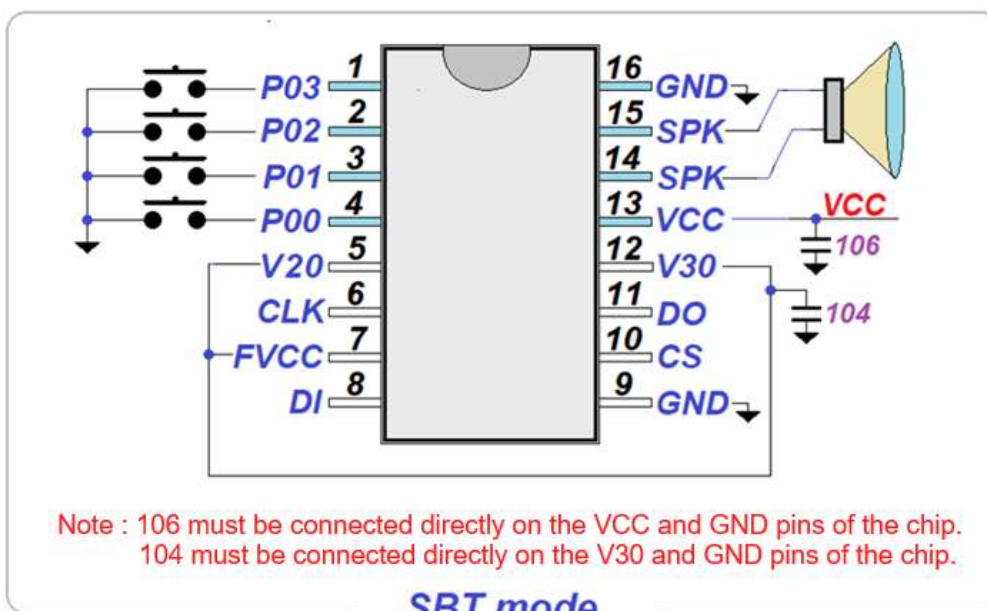
Maximum Voice Groups : 254 for each I/O. All I/O can be chosen input or output. Each Voice Group can have its independent trigger options (See Fig. 1,2,4 and 5 ). SBT mode has an additional on/off function. (See Fig. 7 ).

P00	P01	P02	P03
SEQ/VOL/OUT	SEQ/VOL/OUT	SEQ/VOL/OUT	SEQ/VOL/Reset/OUT

**SEQ :** Sequential Play (See Fig. 3 and 6).

**VOL :** Volume Control

**Output :** BusyH , BusyL , 3Hz , 6Hz , LED-dyna , StopH , StopL



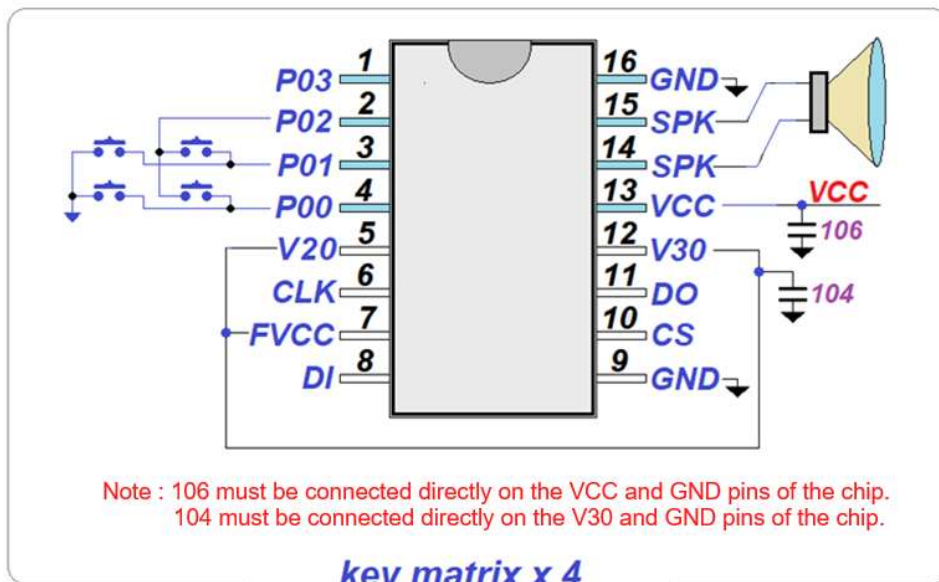
**2. Key matrix mode :**

The sound group is triggered by combining P00 to P03 and GND in a matrix. All I/O scan is chosen input or output. Each Voice Group can have its independent trigger option (see Figures 1, 2, 4 and 5 ).

	<b>P00</b>	<b>P01</b>	<b>P02</b>	<b>P03</b>	<b>keyN</b>
<b>4 mkey</b>	scan in	scan in	scan out	Vol/Reset/Out	mkey1~mkey4
<b>6 mkey</b>	scan in	scan in	scan in	scan out	mkey1~mkey6

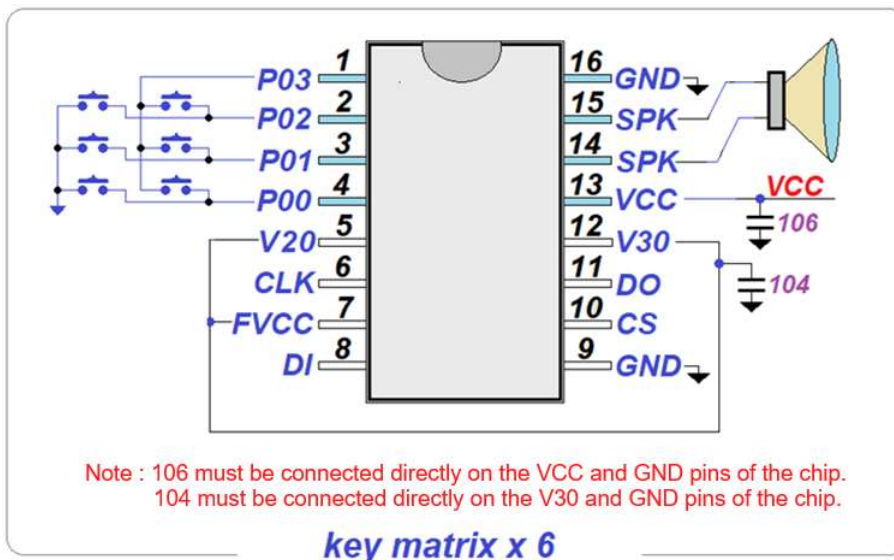
**Output :** BusyH , BusyL , 3Hz , 6Hz , LED-dyna , StopH , StopL

**VOL :** Volume Control



**Ps : p03=input = reset**

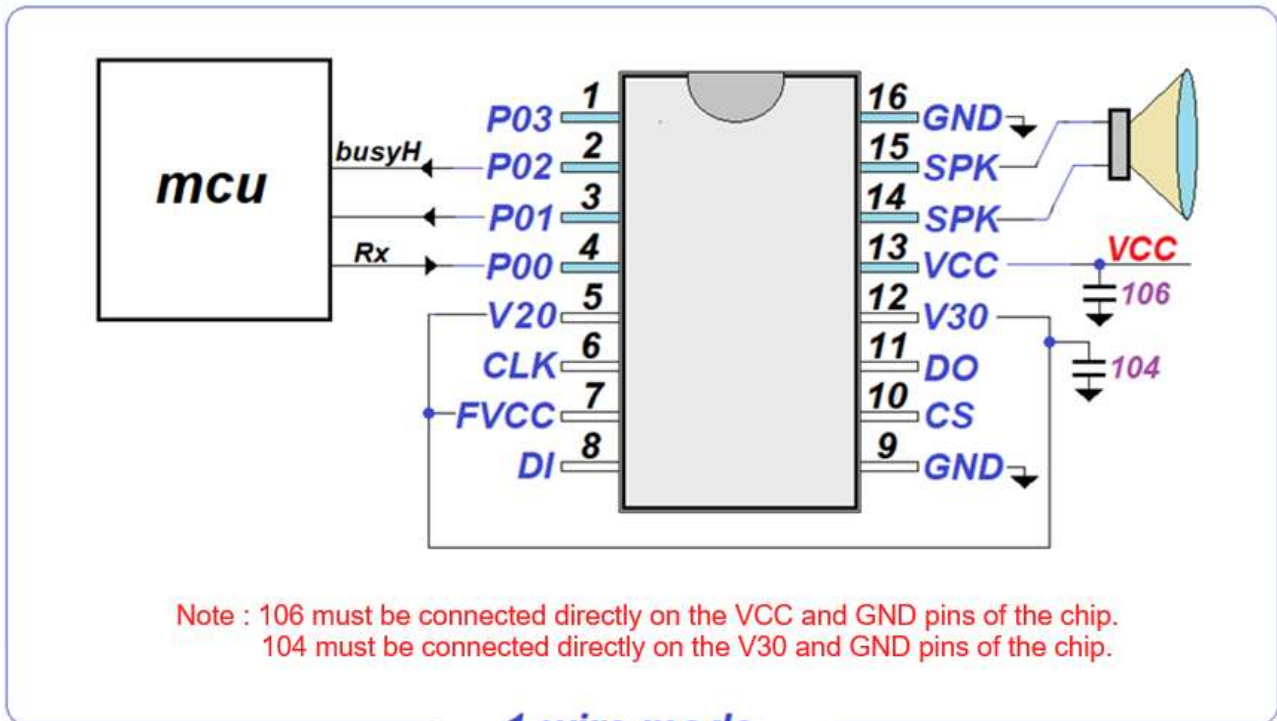
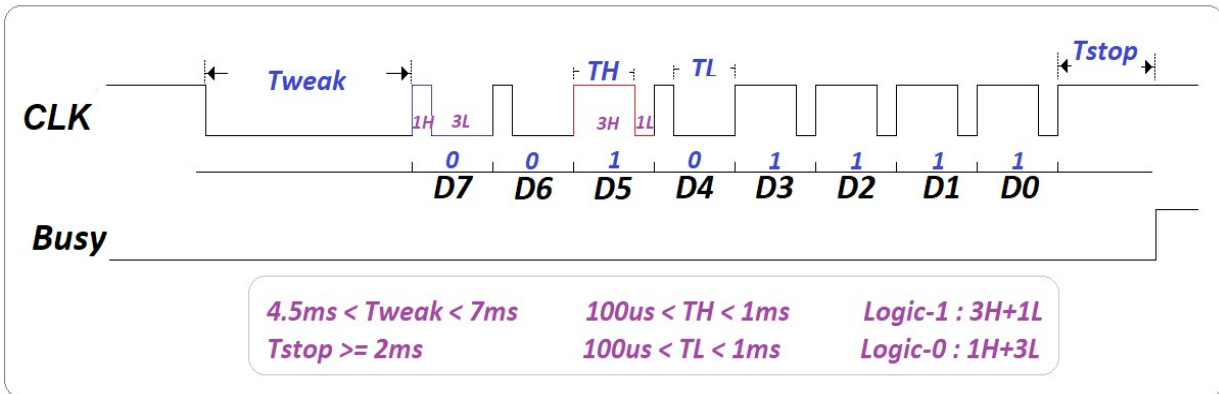
**P03 = output option = busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL**



**3. 1-wire mode :**

<b>P00</b>	<b>P01</b>	<b>P02</b>	<b>P03</b>
<b>Rx</b>	<b>Out</b>	<b>Out</b>	<b>Out/Reset</b>

**Out option : busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL**  
**P03 = input = reset option**

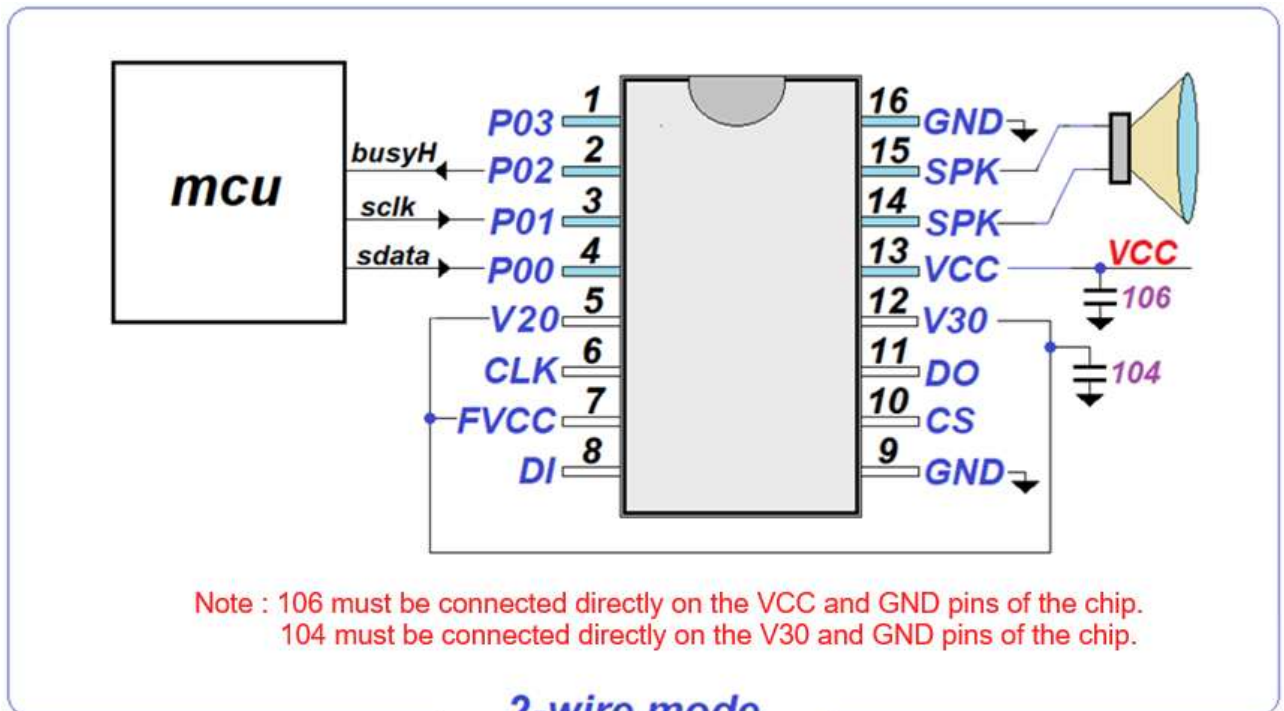
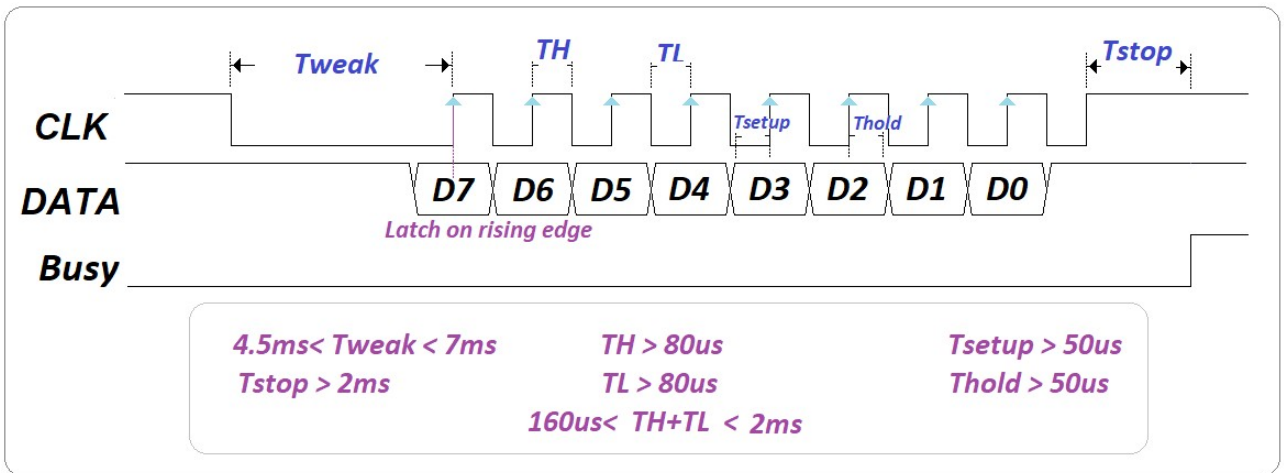


**4. 2-wire mode :**

P00	P01	P02	P03
sdata	sclk	Out	Out/Reset

Out option : busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL

P03 = input = reset option



Note : 106 must be connected directly on the VCC and GND pins of the chip.  
104 must be connected directly on the V30 and GND pins of the chip.

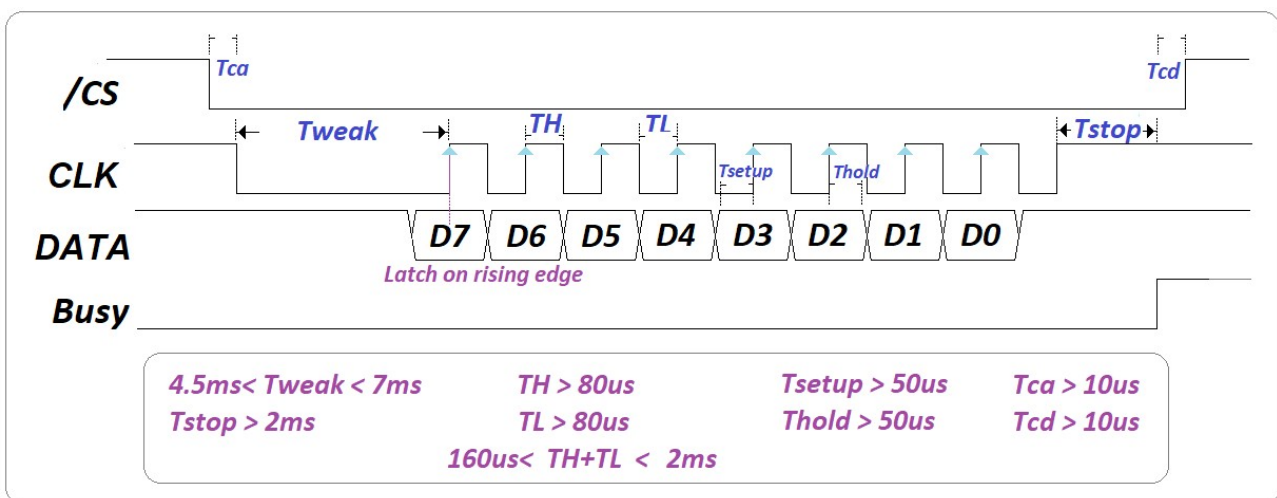
**2-wire mode**

**5. 3-wire mode :**

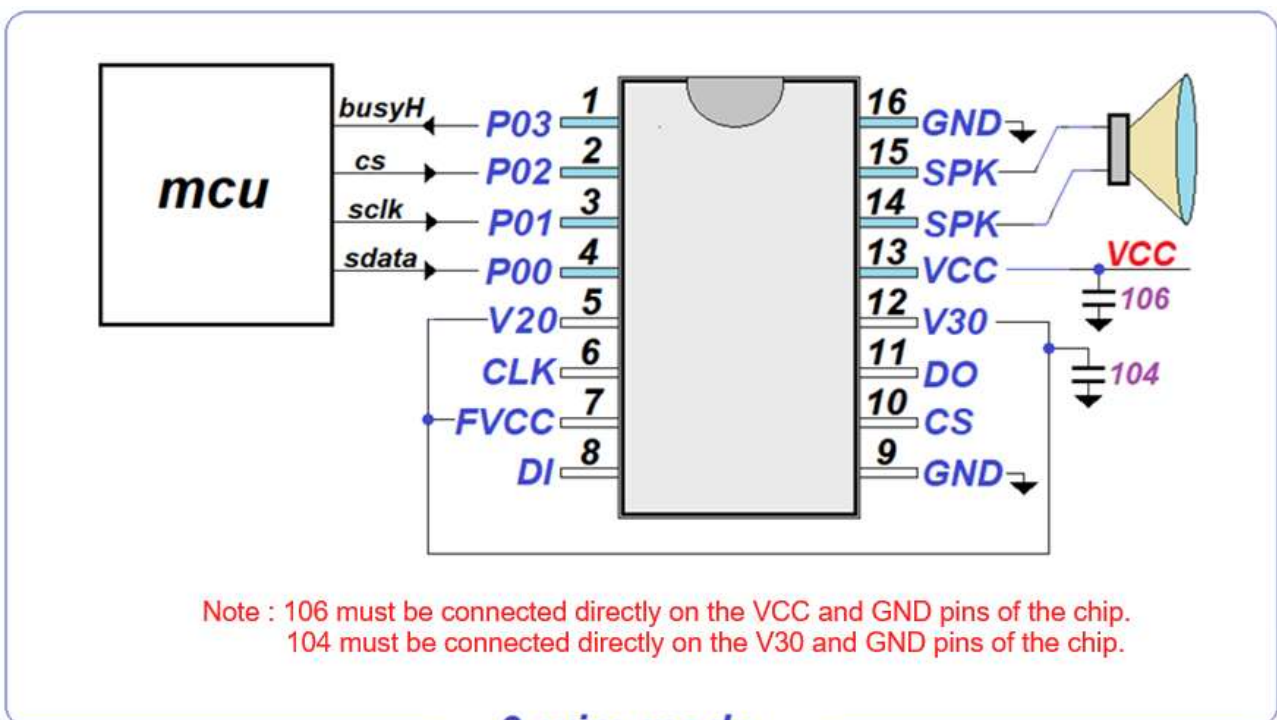
P00	P01	P02	P03
sdata	sclk	Cs	Out/Reset

Out option : busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL

P03 = input = reset option



$4.5ms < T_{week} < 7ms$        $T_H > 80\mu s$        $T_{setup} > 50\mu s$        $T_{ca} > 10\mu s$   
 $T_{stop} > 2ms$        $T_L > 80\mu s$        $T_{hold} > 50\mu s$        $T_{cd} > 10\mu s$   
 $160\mu s < T_H + T_L < 2ms$



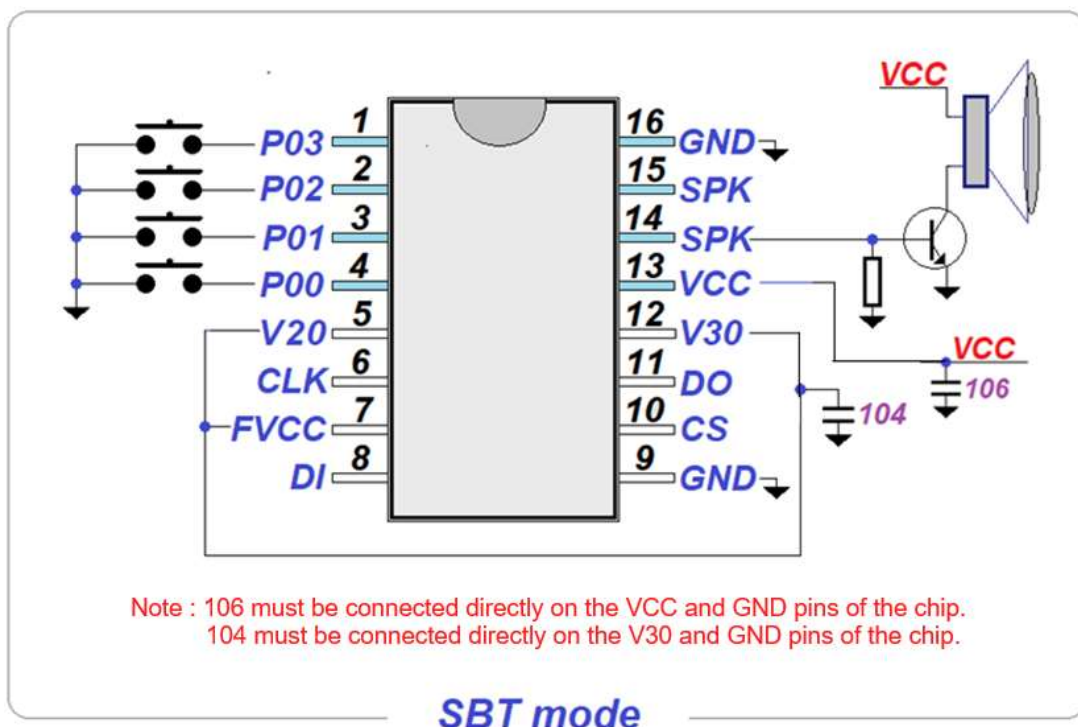
Note : 106 must be connected directly on the VCC and GND pins of the chip.  
 104 must be connected directly on the V30 and GND pins of the chip.

**3-wire mode**

**Command :**

command	D7	D6	D5	D4	D3	D2	D1	D0
play sentence(n)	01 ~ DF							
set volume (n)	E				N ( 0~15 )			
reserved	F0 ~ F7							
repeat off	F8							
repeat on	F9							
Vol-	FA							
Vol+	FB							
Play Next	FC							
Play Next	1	1	1	1	1	1	0	0
Play Previous	FD							
Pause / Resume	FE ( Available in PWM mode only )							
Stop	FF							

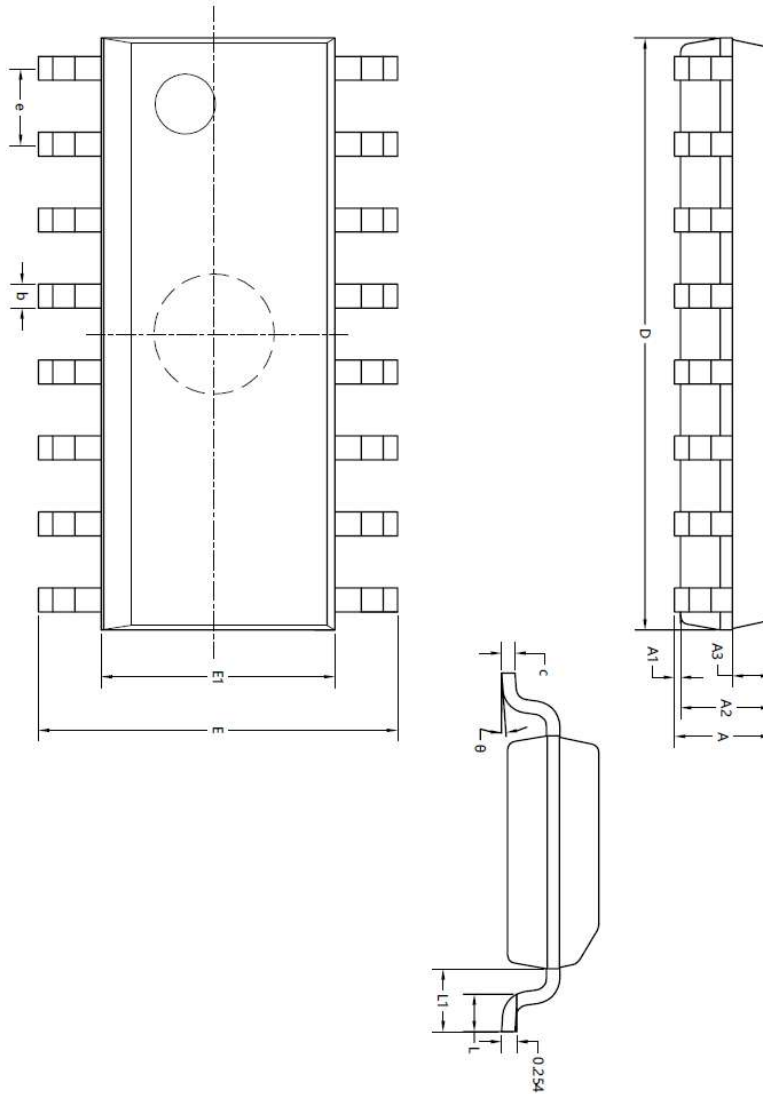
● **DAC Application :**



**■ DC CHARACTERISTICS (VCC = 3.0V , VDD = 2.0V , GND = 0V , TA = 25 °C)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
PORT0[7:4] PORT0[2:0]	Driving Current(VCC · LDO3V)	1.7		4.8	mA	VOH=2.7
PORT0[3]	Driving Current		1.7		mA	VOH=2.7
SPK_P/SPK_N	Driving Current			200	mA	RL = 8Ω @3.0V
SPK_P/SPK_N	Driving Current			320	mA	RL = 8Ω @4.5V
SPK_P	Current DAC output current			3.52	mA	@4.5V
PORT0[7:4] PORT0[2:0]	Sink Current	2.4		13	mA	VOL=0.3
PORT0[3]	Sink Current		2.5		mA	VOL=0.3
SPK_P/SPK_N	Sink Current			200	mA	RL = 8Ω @3.0V
SPK_P/SPK_N	Sink Current			320	mA	RL = 8Ω @4.5V
I_STD	Standby Current		1	6	uA	<2uA @<4.5V <3uA @4.5~5.1V
V20	output Voltage		2.0		V	
	output Current			60	mA	
	output Current		1		mA	
V30	output Voltage		3.0		V	
	output Current			30	mA	80mA @4.5V
	output Current		1		mA	

▪ **Package : SOP16**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.278SC		
L	0.50	0.60	0.70
L1	1.058SC		
θ	0°	4°	8°

## History

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23 July 2024

Internal Initial APLUS Release.

01 April 2025

Modify Page.11 Command Table set volume (n) 0E→E

25 May 2026

Modify Page.11 command table.

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